A SURVEY OF ANALOG-TO DIGITAL CONVERTERS FOR RADAR APPLICATIONS

Technical Report TR-10

R. C. Hicks

Technical Panel KPT-3
(Radar Signal Processing)

Subgroup K
The Technical Cooperation Program

May 1991

97-04-2499

ACKNOWLEDGEMENTS

The author would like to express his appreciation to Mr. Richard Mason and Ms. Donna McQuiston who assisted in surveying the U.S. analog-to-digital converter market and to Mr. Roy Eames of the Royal Signals and Radar Establishment in the United Kingdom for information on analog-to-digital converters from European sources. The author would also like to thank Dr. Mike Story of Data Conversion Systems in Cambridge, England for the informative letter on oversampling converters.

CONTENTS

I. INTRODUCTION 3

II. ANALOG-TO-DIGITAL CONVERTER SURVEY 3

III. ADC CHARACTERIZATION FACILITIES 11

IV. ADC ERROR COMPENSATION TECHNIQUES 15

V. OVERSAMPLED NOISE SHAPING ADCS 18

REFERENCES 20

I. INTRODUCTION

The ever increasing speeds and dynamic ranges of modern radar signal processors require the use of state-of-the-art Analog-to Digital Converter (ADC) technology. In fact, many radar designs are constrained by the lack of ADCs with sufficient speed and/or dynamic range. Several trends in modern radar design are now stressing ADC technology more than ever. For example, the multiple adaptive beams of some phased array radars are now being formed by the radar signal processor. In this arrangement one or two ADCs are required for each element or subarray of the antenna. This huge increase in the required number of ADCs per radar now makes the size, power, and cost of an ADC critically important. Furthermore, the desire to sample at radar IF frequencies to digitally compute the in-phase and quadrature baseband signals can increase ADC speed requirements by 400% or more. The higher bandwidth waveforms sought by some radar designers will also raise ADC speed requirements. Coupled with these new ADC speed requirements is the requirement for more ADC dynamic range to enable processors to detect reduced signature targets in heavy clutter and ECM environments. As a result of these trends in modern radar design, renewed attention has been focused on ADC technology as it is critical to overall system performance.

The primary purpose of this report is to present the results of a survey of state-of-the-art ADCs that was conducted in September of 1990. ADC technology surveys were also conducted in 1978 and 1981 by KTP-3 [1,2]. Current state-of-the-art ADCs (1990 vintage) are graphically compared in this report to the best ADCs of 1978 and 1981 as well as to the ADCs expected by 1992. This should help quantify the progress that has been made in ADC technology over the last decade and enable the reader to estimate the pace of future ADC technology progress. Additional topics include ADC characterization facilities, ADC error compensation techniques, and oversampled noise shaping ADCs.

II. ANALOG-TO-DIGITAL CONVERTER SURVEY

The information on currently available ADCs was obtained by an exhaustive telephone survey of known ADC vendors, journal articles, and advertising literature [3,4]. The ADCs chosen for this report have sample rates ranging from 100 kHz to 500 mHz and word lengths of 6 to 18 bits. A vendor may feature several ADCs of the same word length but with various maximum sample rates. Only the vendor's fastest ADC at each word length was included in this report. ADCs were also excluded from this report if their sampling rates were less than one-tenth of the industry average sample rate of ADCs with the same word length. Information on ADCs meeting these criteria was obtained from the 25 manufacturers listed in Table 1.

TABLE 1. ANALOG-TO-DIGITAL CONVERTER MANUFACTURERS

1. Advanced Analog
2. Analog Devices
3. Analogic
4. Burr-Brown
5. Catalyst Semiconductor
6. Comlinear
7. Crystal/Gould
8. Datel
9. DCS
10. DCS/STL
11. ILC Data Device
12. ITT
13. MEDL
14. Micro Power Systems
15. MicroNetworks
16. Motorola
17. Panasonic
18. Plessey
19. Siemens
20. Sipex
21. Sony
22. STC
23. Tektronix
24. TRW
25. Westinghouse

A graphical presentation of the ADCs available in 1990 is shown in Figure 1. The word length in bits is plotted against the maximum sampling rate in units of Mega Samples Per Second (MSPS). The data points of Figure 1 are surrounded by a performance envelope which will be used in later figures to show ADC technology progress. The manufacturer's name, part number, and maximum sampling rate of these ADCs are listed in Table 2. The ADCs in Table 2 without part numbers are non-commercial parts and are generally only for the company's private use.

The maximum sampling rates for this group of ADCs is quite impressive. All of the 6 to 10 bit ADCs have sample rates of 30 MSPS or higher. The fastest ADCs of this group are represented by a 500 MSPS 8 bit ADC from Tektronix and a 500 MSPS 6 bit ADC from Analog Devices. At 20 MSPS, Comlinear has the fastest 12 bit ADC. It is followed by no less than seven 10 MSPS 12 bit ADCs. Analog Devices now has a 14 bit ADC at the 10 MSPS rate. Also, 15, 16, and even 18 bit ADCs are available at speeds greater than .1 MSPS.

There are two trends in ADC technology that have become more dominant now than in the past. The first trend is the miniaturization of ADCs. Most ADCs suitable for radar applications are now either monolithic or small hybrid packages. In the previous two surveys many of the ADCs were composed of multiple boards or even an equipment rack of boards. Generally, the 6-11 bit ADCs are now monolithic and the 12-18 bit ADCs are hybrids. Most of the ADCs in this survey are smaller than the size of a small board. Thus, today's radar designer often has the option of selecting an ADC more for its performance than by its packaging. The second trend is that many ADCs now include internal sample-and-hold circuitry. The purpose of sample-and-hold circuitry is to instantaneously sample the input voltage and hold it at a constant level while the ADC converts the voltage to a digital representation. Therefore unlike previous surveys, this report does not include a survey of stand-alone sample-and-hold devices.

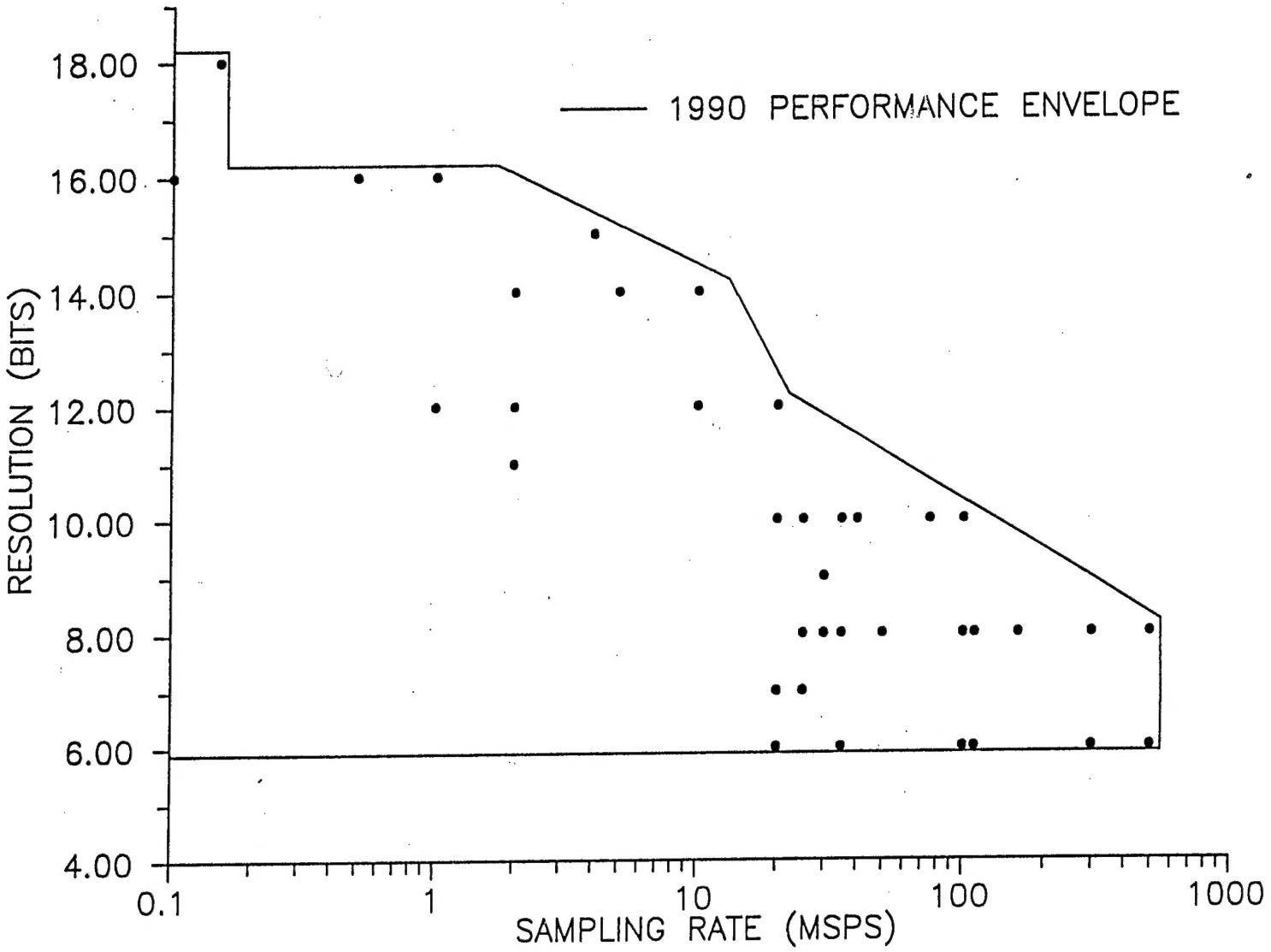

FIGURE 1. 1990 A/D CONVERTERS

TABLE 2. 1990 ANALOG-TO-DIGITAL CONVERTERS

RESOLUTION (BITS)	MANUFACTURER/PART NUMBER		MAXIMUM SAMPLING RATE (MSPS)
18	Analogic	ADC5020	.144
16	Analogic	ADC4344	1.0
16	Burr-Brown	ADC701	.5
16	Datel	ADS930	.5
16	Analog Devices	AD1377	.1
15	Westinghouse	N/A	4
14	Analog Devices	AD9014	10
14	Westinghouse	N/A	5
14	Analogic	ADC3110	2
14	Datel	ADS942	2
12	Comlinear	CLC936	20
12	Analog Devices	AD9005	10
12	Burr-Brown	ADC603	10
12	Datel	ADS130	10
12	ILC Data Device	ADC-00110	10
12	MicroNetworks	MN6300	10
12	Sipex	SP9560	10
12	TRW	TH1202	10
12	Catalyst Semiconductor	CAT5412	2
12	Advanced Analog	ADC5245	1
12	Crystal/Gould	CS5412	1
11	Micro Power Systems	MP7685	2
10	Tektronix	N/A	100
10	Analog Devices	AD9060	75
10	Micro Networks	ASA1040	40
10	Panasonic	AN6869	35
10	Comlinear	CLC920	25
10	Datel	ADC310	20
10	TRW	TDC1020	20
9	TRW	THC1049	30
8	Tektronix	TKAD10C	500
8	Analog Devices	AD9038	300
8	Sony	CXA1176AK	300
8	Datel	ADC 32/33	160
8	Plessey	SP97508	110
8	Micro Networks	MN5901	100
8	Siemens	SDA 8010	100
8	Sipex	SP1078	50
8	TRW	TDC1025	50
8	Micro Power Systems	MP7688	35
8	Panasonic	AN6857	35
8	ITT	UVC3130	30
8	Motorola	MC10319	25
7	Motorola	MC10321	25
7	Datel	ADC207	20
7	TRW	TDC1047	20
6	Analog Devices	AD9006	500
6	Micro Networks	MN5900	300
6	Siemens	SDA8200	300
6	Plessey	SP9756	110
6	TRW	TDC1029	100
6	Micro Power Systems	MP7686	35
6	Panasonic	AN6856	35
6	Datel	ADC-207	20
6	Sony	CXD1172	20

As part of the survey, manufacturers were asked to predict the new ADC products that they were likely to produce in the next 12 to 18 months. The ADCs that are close to or exceed the 1990 performance envelope are shown in Figure 2. The number of manufacturers independently working to produce an ADC with the same specifications is shown in parentheses, if more than one is involved. Manufacturer names are not listed as anonymity was often requested. Exciting 1992 ADC projections include a .1 MSPS 24 bit ADC, a 10 MSPS 16 bit ADC, a 30 MSPS 14 bit ADC, a 250 MSPS 10 bit ADC, and a 1000 MSPS 7 bit ADC.

In order to illustrate the technology progress of the last decade, the ADC performance envelopes of 1978, 1981, and 1990 were plotted in Figure 3. The 1978 and 1981 performance curves were determined by the best monolithic, hybrid, and small board based ADCs as reported by the earlier KTP-3 surveys. Very measurable progress in speed and resolution can be observed from Figure 3. Figure 3 shows that the most dramatic progress for the three years between 1978 and 1981 occurred for the 8 to 12 bit ADCs. During the 9 years between 1981 and 1990 the most progress was made in the 12 to 18 bit ADCs.

Table 3 lists the ADCs that have been technology benchmarks in the past as well as those of 1990 and those projected for 1992. Table 3 gives the speed in MSPS of the fastest ADCs of the years of 1978, 1981, 1990, and 1992. Each ADC listed represents the fastest ADC available for its resolution and year. In addition, a listed ADC had to be faster than all ADCs of greater resolutions. The large multiboard ADCs of 1978 and 1981 are listed separately in the last two columns. The multiboard ADCs were excluded from the technology progress comparisons of the first four columns as their performance is determined as much by size and cost allocations as by their monolithic and hybrid ADC technology. Where applicable, the percentage increase in speed of an ADC compared to the previous column is given in parenthesis. The average of these percentage increases in speed for each year is given near the bottom of the table. The average annual percentage rate of speed increase is shown at the bottom of Table 3. It is interesting to note that during the latest period of time, 1981 to 1990, the average yearly increase in ADC speed was only 17%. In contrast, the average yearly increase in speed during the 1978-1981 period was 135%. The low 17% growth rate would have been worse if this survey had been conducted in 1987. In fact this survey was purposely delayed after a preliminary 1987 survey showed a surprising lack of ADC development progress. [5] Delaying this survey until 1990 accommodated several recent ADCs which have significantly advanced the state-of-the-art. If the 1992 predictions are correct, a large average yearly speed increase of 124% will be experienced between 1990 and 1992. This would reverse the trend of declining progress in ADC technology development experienced between 1981 and 1987.

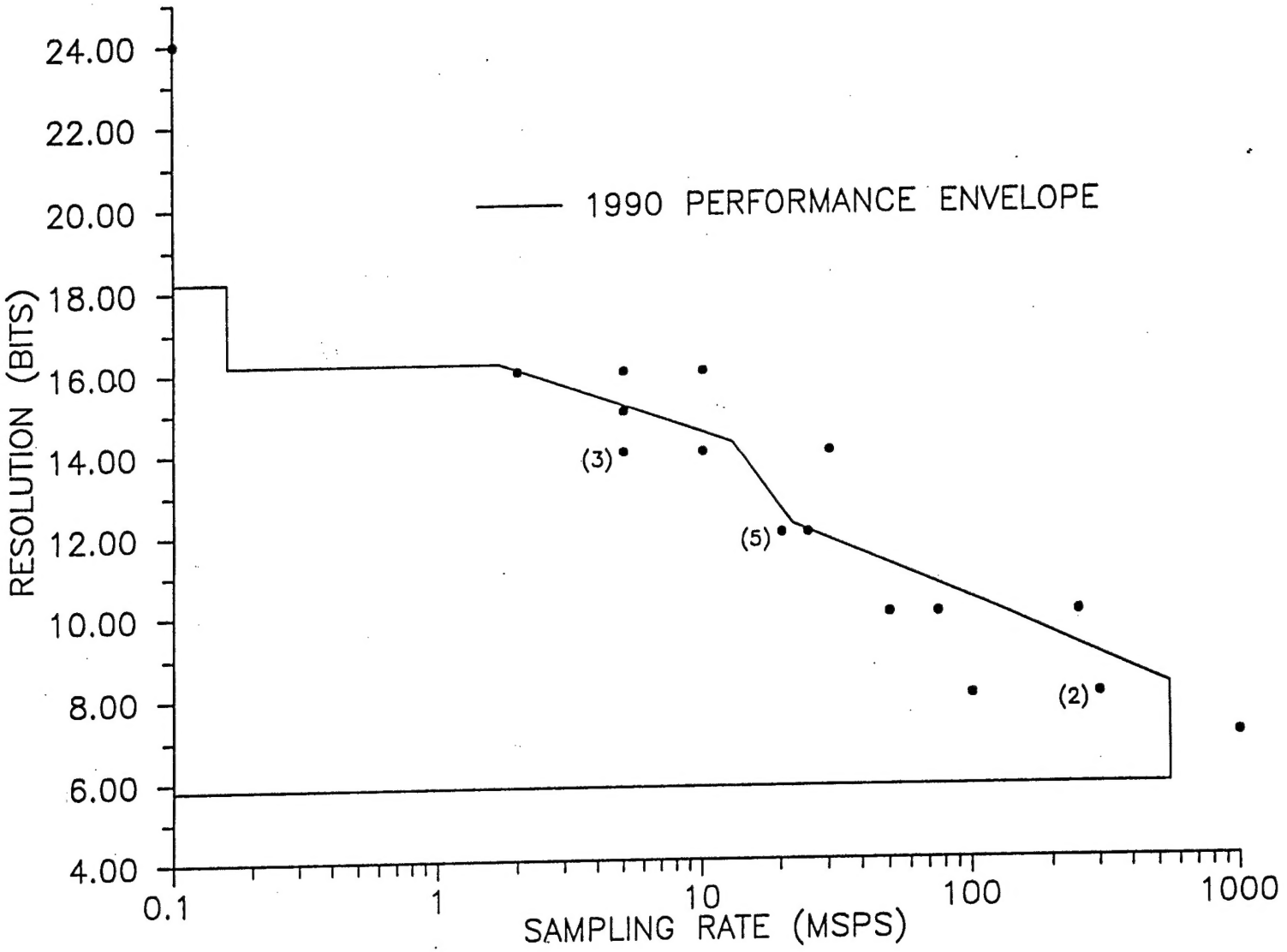

FIGURE 2. 1992 A/D TECHNOLOGY PROJECTION

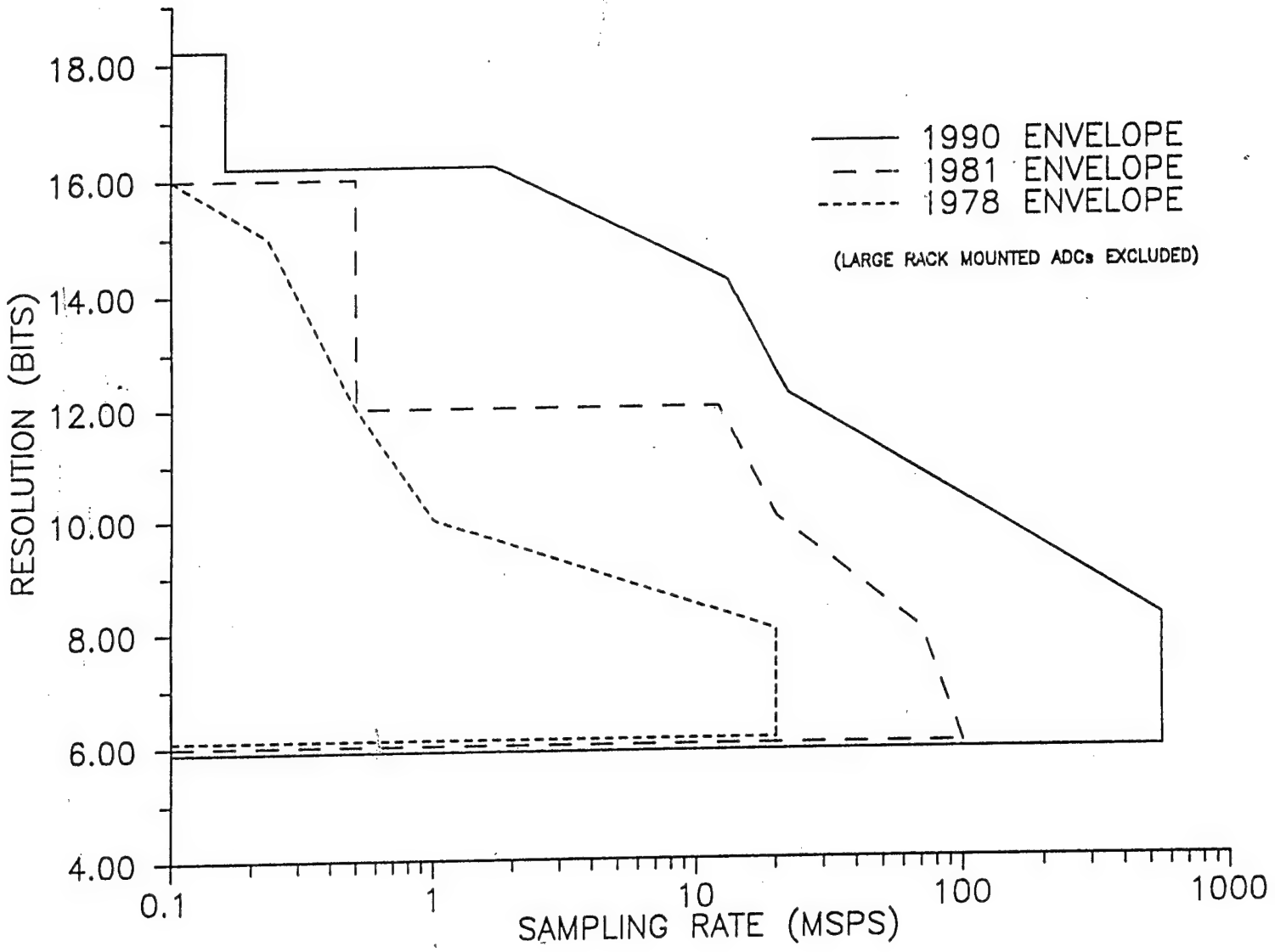

FIGURE 3. A/D CONVERTER DEVELOPMENT HISTORY

TABLE 3. A/D CONVERTER TECHNOLOGY PROGRESS

Resolution (bits)	1978 (MSPS)	1981 (MSPS)	1990 (MSPS)	1992 (MSPS)	1978 MULTIBOARD (MSPS)	1981 MULTIBOARD (MSPS)
24				.10		
18			.14			
16	.10	.50(400%)	1.0(100%)	10(900%)		
15	.23		4.0		.70	1.0
14			10	30(200%)		
13					10	10
12	.50	12(2300%)	20(70%)			
10	1.0	20(1900%)	100(400%)	250(150%)		
8	20	70(250%)	500(610%)		100	
7				1000		
6		100			500	
AVG SPEED INCREASE		1200%	300%	400%		
AVG ANNUAL SPEED INCREASE		135%	17%	124%		

III. ADC CHARACTERIZATION FACILITIES

ADC specifications traditionally published by ADC manufacturers include maximum sampling rate, signal-to-noise ratio (SNR), gain error, linearity error, offset error, missing digital output states, and numerous others.[6,7,8] The definition and testing methods for these ADC specifications is well documented. Unfortunately, the performance specifications are often a measure of the static performance of an ADC. The static performance is a measure of the difference between actual and theoretical ADC output of a non-changing input.

For radar applications, however, the dynamic performance is more important to characterize than the static performance.[9] Dynamic performance is a measure of how accurately an ADC performs when the input is rapidly changing. Dynamic errors are generally a function of sampling rate, bandwidths of the ADC input signals, and the time jitter associated with the sample-and-hold circuitry. Although good static performance is important, it does not guarantee satisfactory dynamic performance. Good dynamic performance however, does imply good static performance.

When the performance of a new or state-of-the-art ADC is critical to a radar application, the ADC should undergo independent dynamic testing. This is due in part because an ADC manufacturer cannot test and characterize each ADC for the diverse application peculiarities and requirements that exist. Unfortunately, the increased speed and dynamic range of state-of-the-art ADCs has made independent dynamic testing very difficult. For example, most readily available laboratory signal sources do not have an adequate SNR or low enough harmonic content to test even a 12-bit ADC.[7]

To meet the need for independent and rigorous testing several dedicated ADC test facilities have been established. The Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Massachusetts and the GEC-Marconi Research Centre in Chelmsford, England each operate a dedicated test facility for the dynamic characterization of state-of-the-art ADCs. Both facilities have tested state-of-the-art ADC prototypes for well known ADC manufacturers. In addition, various ADC users have contracted with these facilities for independent and customized testing of state-of-the art ADCs.

The Lincoln Laboratory ADC characterization facility specializes in dynamic testing of very fast ADCs with very large dynamic ranges.[9,10] A typical configuration for their tests is shown in Figure 4. Lincoln dumps the ADC output into a high performance computer without the use of digital-to-analog converters (DACs) which could mask the true performance of the ADCs. The high speed data buffer can store 128k contiguous 16-bit samples at clock rates up to 250MHz or 256k contiguous 8-bit

samples at a 500MHz rate. As shown by Figure 4 the input to the ADC can be two sinusoids or a sinusoid plus noise. The ADC input is kept pure by a signal conditioner that employs 90dB stopband filters to remove harmonics and to prevent aliasing. In order to isolate phase-noise and jitter effects to the ADC, the signal generators shown have a phase-noise performance equal or better than -130 dBc/Hz at 20kHz from the carrier. These inputs may also be monitored by a spectrum analyzer or noise receiver as shown. The test frequencies and sample clock rates are kept stable and free of phase noise by using a 10MHz reference with a stability of $3X10^{-10}$ parts per day.

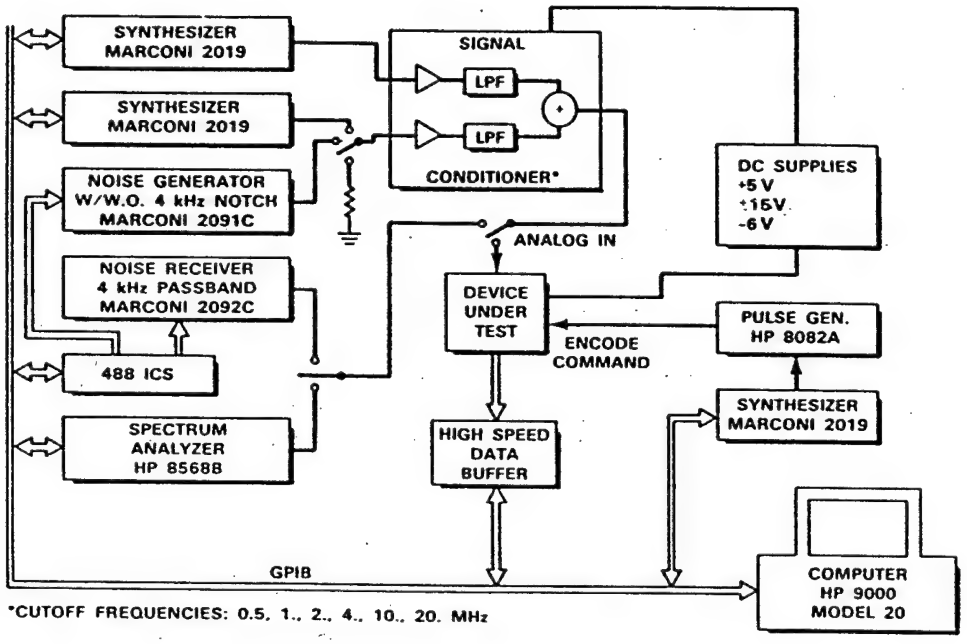

FIGURE 4. Lincoln Laboratory ADC Characterization Configuration

To check the linearity of the ADC under test, a histogram is formed from the ADC data. The x-axis of the histogram represents all the possible digital output codes and the y-axis records the number of occurrences of each output code. This histogram is then compared to the theoretical histogram of an ideal ADC with the same input. This ideal histogram is simply the probability density function of the input waveform. Nonlinearity in an ADC is caused by nonuniform quantization intervals. A quantization interval that is longer than normal will cause too many occurrences to show up in the histogram at that code. Conversely, a shorter than normal quantization interval will result in not enough occurrences. Any completely missing ADC code outputs will cause an obvious null in the histogram.[10]

The bulk of the ADC testing is performed by analysis of an FFT produced spectrum of the ADC output data. Figure 5 shows the power spectrum resulting from a single sinusoidal input. As shown in Figure 5, the spurious-free dynamic range (SFDR) is defined as the difference in dB between the fundamental power level and the power level of the highest noise spur. The quantity P_{qf} denotes the average quantization noise power present in each FFT frequency cell. The SFDR is a good measure of useful dynamic range. The SFDR is typically characterized for a wide range of input power levels, sampling rates and fundamental frequencies.[10]

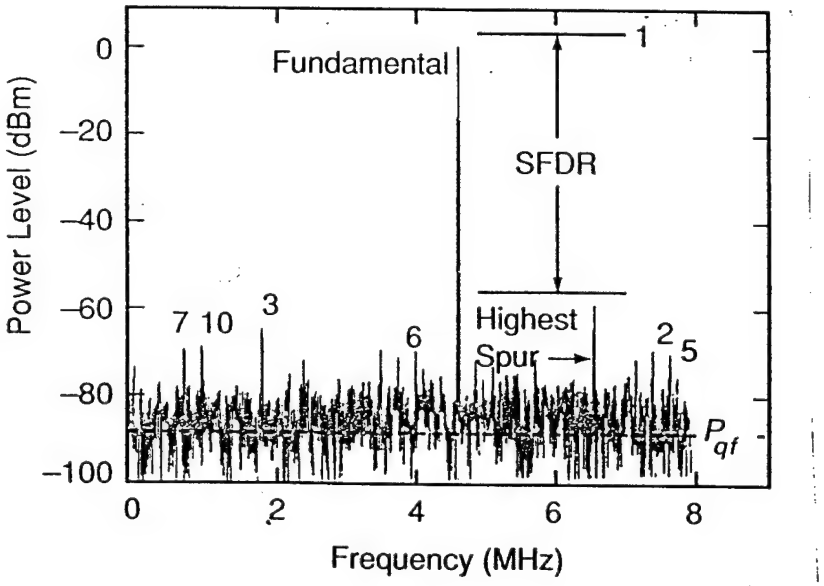

FIGURE 5. Power Spectrum from Lincoln SFDR Test

The dynamic performance of an ADC that is expected to see a large number of simultaneous signals is characterized by a noise power ratio (NPR) test. For this test Lincoln generates noise with a flat spectrum up to a cutoff frequency that is less than half the sampling frequency. A notch filter then produces a very deep null over a small portion of the frequency band. The output power spectrum of the ADC resulting from the notched input is shown in Figure 6. As shown in the figure, the NPR is defined as the ratio of the power spectral density inside the notched frequency band to the power spectral density outside the notch. An ideal ADC with infinite word length would faithfully reproduce the notched input noise spectrum. For a real ADC, the notch and the NPR is limited by the SFDR of the ADC. Thus, the NPR serves as an additional measure of ADC linearity.[10]

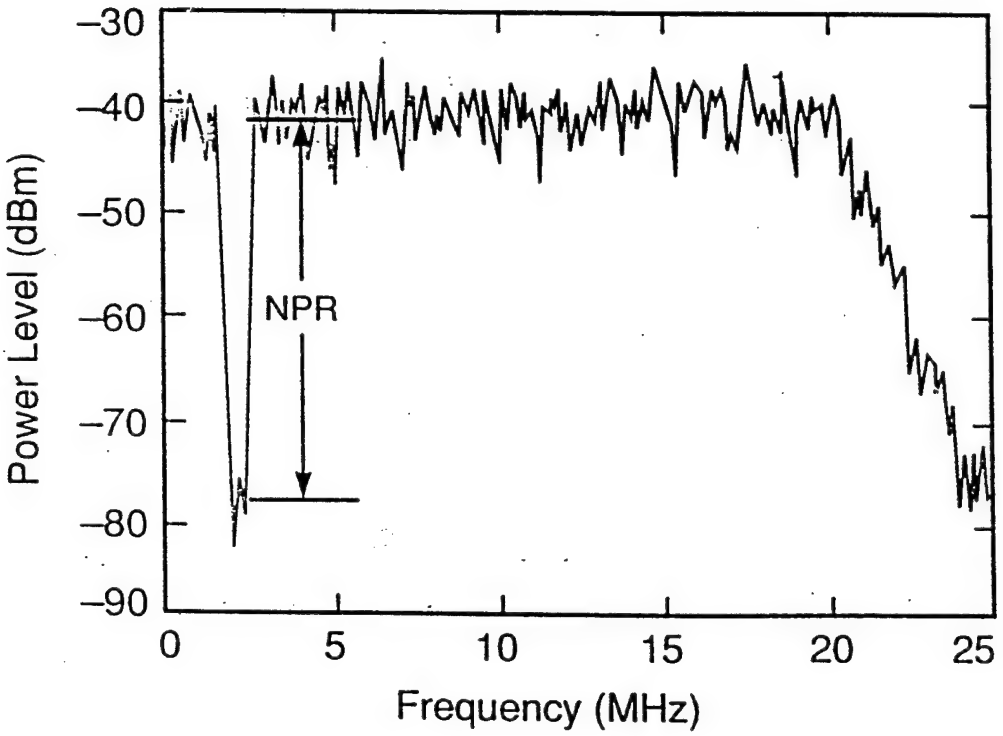

FIGURE 6. Power Spectrum Form Lincoln NPR Test

The GEC-Marconi facilities and test procedures are typified by their test of the Tektronix TKADZOC 8-bit, 250MHz ADC.[11] For this testing GEC-Marconi designed and built a very high quality evaluation board which sought to minimize external noise sources while maintaining the full 250MHz sampling rate. GEC-Marconi generated the differential clock input required by the Tektronix ADC and provided a very pure analog sinusoidal input signal. Similar to Lincoln Laboratories, the digital ADC output was stored in real time in a special purpose high speed memory, before being off loaded into a general purpose computer. FFT based spectral analysis of the data was then performed to determine the power in the signal, harmonic, and dc components as well as the noise floor. From this information the effective number of bits was calculated. The effective number of bits is defined as the number of bits required by an ideal ADC to equal the measured SNR of the tested ADC. The linearity of the ADC was characterized from analysis of spectral components as well as by histogram testing. This dynamic testing was accomplished over various stressing combinations of different sampling rates, signal amplitudes and signal input frequencies.

IV. ADC ERROR COMPENSATION TECHNIQUES

Lincoln Laboratory has recently investigated post sampling error correction techniques that could be used to decrease the harmonic distortion found in high speed, high resolution ADCs.[9,10,12] The basic approach of their compensation techniques is to build a two-dimensional look-up table of the measured ADC errors resulting from all expected amplitudes of a fixed frequency sinusoid. The ADC output sample coupled with information from previous outputs is used to generate the look-up table address for the appropriate error correction factor. The stored error is then subtracted from each ADC output sample.

Lincoln's initial efforts focused on using the slope of the incoming sinusoid as well as the ADC output sample value to address a two-dimensional error correction table.[12] The slope of the incoming sinusoid is an indicator of its amplitude. Figures 7 and 8 show the power spectrums of an uncompensated and a compensated Analog Devices MOD-1205 (12 bit, 5MHz) ADC. The line marked P_{FS} is at the full scale power level of the ADC, P_Q is at the quantizing power level, and P_{QF} is below the quantizing power level by the FFT processing gain. Figures 7 and 8 show a dramatic 30dB reduction of the harmonic spurs. This compensation was achieved with a 256 X 128 point error calibration table optimized for the 497kHz input sinusoid. The sample rate was 4.096mHz.

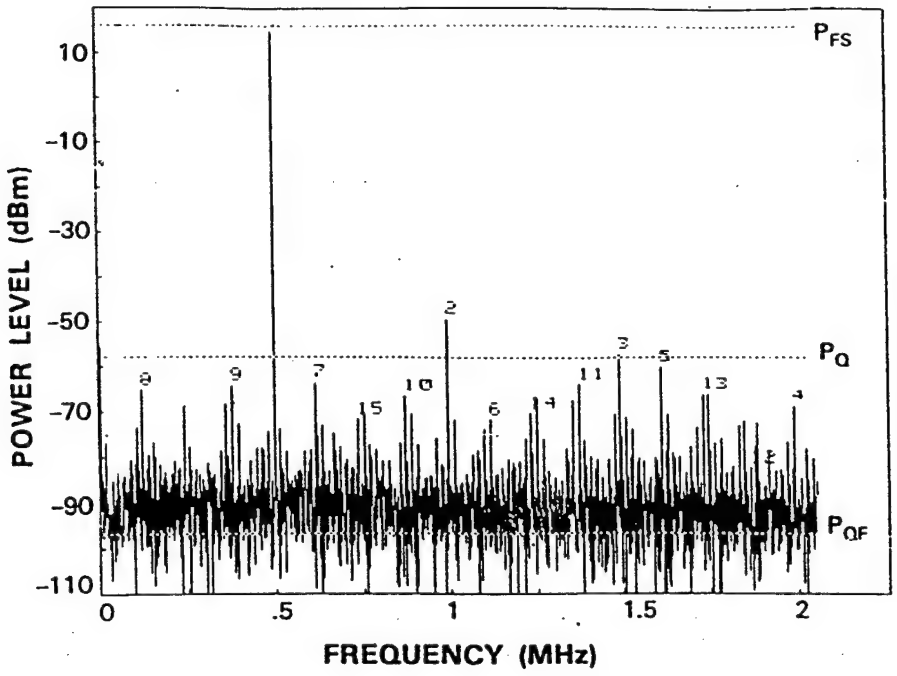

FIGURE 7. FFT Spectrum (16384 Points) of a Full Scale Tone at 497kHz Before Compensation.

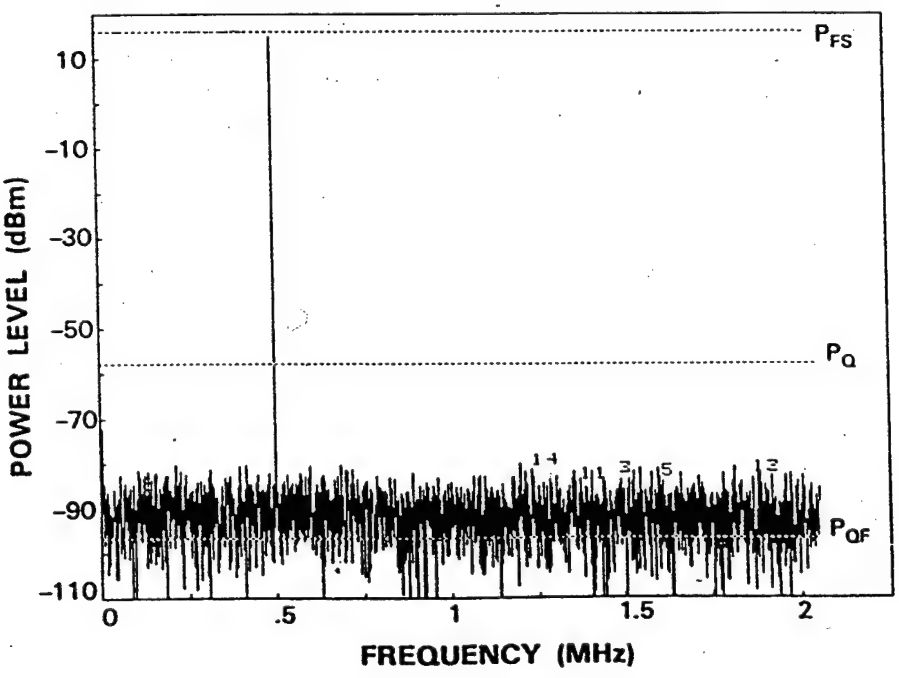

FIGURE 8. FFT Spectrum After Compensation of Same Tone as Above.

Figure 9 shows the SFDR of the MOD 1205 ADC resulting from a 491KHz input sinusoid at varying power levels. In this figure the uncompensated performance is compared to the compensated performance resulting from different correction tables. As expected, the compensation performance falls off as the input frequency becomes mismatched to the frequency used to derive the error correction table.

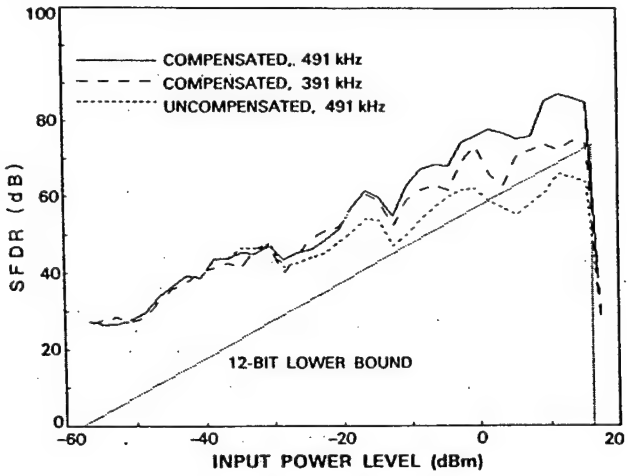

FIGURE 9. SFDR Curves for Compensated and Uncompensated MOD-1205 ADC for 491kHz Input Sinusoid.

Later Lincoln work focused on state space representation (SSR) compensation techniques.[10] In this approach, the same error correction table used to generate Figure 8 is addressed simply by the current and previous ADC output. This results in a much simpler implementation as the slope no longer has to be estimated.

There are, however, several disadvantages of the current techniques.[10] One disadvantage is that the compensation procedure only works well for input sinusoids with a frequency of one-fourth the sampling rate or less. Also, as shown by Figure 9, the optimum benefit of the technique could be limited to a bandwidth of less than one-fourth of the sampling rate. In addition, the technique is only practical for ADCs whose error characteristics are stable over temperature and time. These shortcomings are acknowledged by Lincoln and are influencing future research into error compensation techniques.

These compensation techniques may be more suitable to applications involving relatively large sinusoids of a known or narrow band of frequencies. Unfortunately, radar applications generally lack these characteristics. Nevertheless, error compensation techniques may eventually be developed that are useful for maximizing the usable dynamic range of an ADC in a radar application.

V. OVERSAMPLED NOISE SHAPING ADCS

ADCs suitable for radar applications have long been dominated by three basic architectures. The flash architecture, also known as parallel approximation, has dominated the very fast low resolution ADCs. The largest resolution ADCs have typically used the successive approximation or the relatively new multipass architecture.[13] These ADC architectures are not without their problems however. Traditional ADCs typically feature many analog components such as precision analog comparators and voltage dividers. These analog components result in manufacturing problems which only get worse as the ADC resolution increases. In addition, the analog components of the ADCs do not easily scale to smaller dimensions as do the digital components.[14]

A radically different ADC architecture - the oversampling noise shaping ADC (ONSA) avoids many of these problems by replacing much of the analog circuitry with digital circuitry. The delta-sigma ADCs, a special class of ONSAs, take fullest advantage of digital solid state technology resulting in ADCs that are smaller, less expensive, and more stable than conventional ADCs.[14] The delta-sigma ADCs are being made to handle signals from dc to 1MHz with resolutions from 12 to 24 bits. They now dominate the very high resolution, low frequency field (.2Hz to 2 KHz, 20-24 bits) because of their inherent linearity and their ability to eliminate aliasing.[13] ONSAs are also being used in audio, sonar, and communication applications.[14]

The ONSA architecture was developed and analyzed in the 70's and early 80's by Candy,[15] Agrawal and Sheno,[16] and others. The general ONSA architecture is shown in Figure 10.[17] The first stage ONSA consists of a clocked feedback loop containing H(z) (e.g., a one or two pole integrator), a low resolution digital estimator (e.g., an N-bit ADC), and an N-bit DAC. This feedback loop is followed by a decimating digital low pass filter. The sampling rate of the loop, f_1, is at a much higher rate than the output sampling rate f_2. This oversampling factor, f_1/f_2 typically varies from 8 to 256.

The clocked feedback loop produces a coarse estimate of the input signal that oscillates about the true value of input.[17] The N-bit ADC quantizes the difference (delta) between the incoming signal and the sum (sigma) of previous differences. The sigma's difference from sample-to-sample is typically small as the comparison is performed at such a high rate relative to the signal bandwidth. The name delta-sigma ADC is derived from the above explanation and is used to describe an ONSA employing a one-bit digital estimator and DAC.[18]

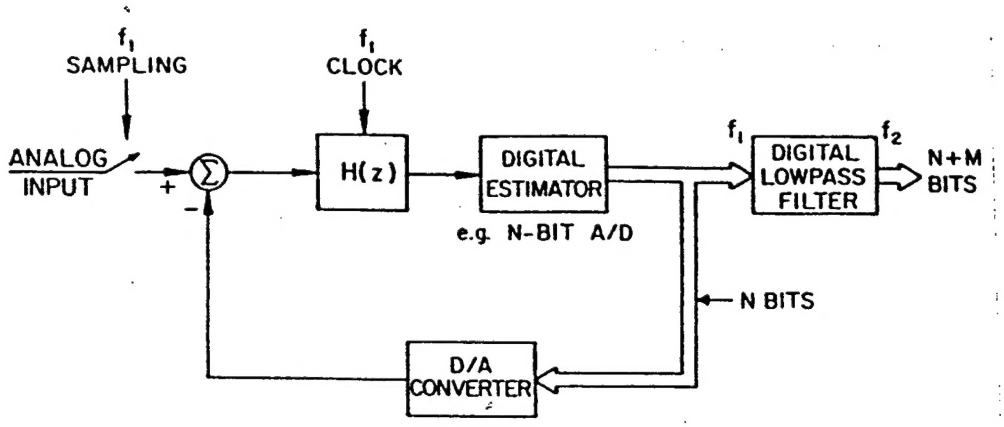

FIGURE 10. Generic ONSA Architecture

The feedback loop of Figure 10 shapes the quantization noise of the digital estimator to minimize the noise in the signal bandwidth, at the expense of the higher frequencies. Therefore, the subsequent bandwidth reduction of the digital lowpass filter reduces the quantization noise by more than the oversampling factor. Typical theoretical SNR enhancements, from the initial N-bit estimates, are [17]

$$\Delta \text{ SNR (dB)} = 9\ L - 5.2 \qquad (1)$$

$$\Delta \text{ SNR (dB)} - 15\ L - 13 \qquad (2)$$

where L is the oversampling factor.

Equations 1 and 2 suggest that the SNR of ONSAs can be increased to whatever levels that are desirable by simply increasing the oversampling factor. However, the linearity and resulting maximum SNR of a ONSA with a multibit ADC and DAC is limited by the accuracy of the DAC transfer function. The single bit DAC of a delta-sigma ADC has only two output levels. As a result any error in these levels produces only a gain error or offset in the overall transfer function of the ADC. The use of multibit ADCs and DACs does, however, reduce the required oversampling factors leading to higher speed ADCs.[17]

Currently, both delta-sigma and multibit ONSAs are being developed and produced for a variety of non-radar applications. Although the ONSAs are not currently fast enough for most radar applications, they do have a growth potential for low speed, very large dynamic range applications.[14]

REFERENCES

1) D. W. Burlage and E. R. Billam, "Survey of Analog-to-Digital Converter Technology for Radar Applications," KTP-3 Technical Report No. TR-1, Apr 78.

2) B. E. Jones, "A Survey of Analog-to-Digital Converter Technology for Radar Applications - Amendment A," KTP-3 Technical Report No. TR-1A, Dec 81.

3) F. Goodenough, "Four Hybrid ADCs Hit New Performance Highs," Electronic Design, 13 Sep 90, pp. 37-42.

4) F. Goodenough, "12-Bit Sampling ADCs Come of Age," Electronic Design, 13 Sep 90, pp. 47-56.

5) R. C. Hicks, "Analog-to-Digital Converters," U.S. Army Missile Command Technical Memo No. AS-88-45, Sep 88.

6) J. R. Naylor, "Testing DA and AD Converters," IEEE Trans. on Circuits and Systems, Vol. CAS-25, No. 7, Jul 78, pp. 526-538.

7) M. W. Johnson, "Test High Speed, High Resolution A-D Converters," Electronic Design, 10 May 90, pp. 95-100.

8) S. K. Tweksbury, et. al., "Terminology Related to the Performance of S/H, A/D, and D/A Circuits," IEEE Trans. on Circuits and Systems, CAS-25, No. 7, Jul 78, pp. 419-426.

9) F. H. Irons, "Dynamic Characterization and Compensation of Analog to Digital Converters," Proceedings of the IEEE International Symposium on Circuits and Systems, San Jose, CA, 5-7 May 86, pp. 1273-1277.

10) D. Asta and F. H. Irons, "Dynamic Error Compensation of Analog-to-Digital Converters," The Lincoln Laboratory Journal, Volume 2, Number 2 (1989), pp. 161-181.

11) M. J. Darcy, "Tektronix TKAD20C Evaluation," GEC-Marconi Research Centre, Report No. Y/232/MJD/89/59, Mar 89.

12) T. A. Rebold and F. H. Irons, "A Phase-Plane Approach to the Compensation of High Speed Analog-to Digital Converters," Proceedings of the IEEE International Symposium on Circuits and Systems, Philadelphia, PA, 4-7 May 87, pp. 455-458.

13) F. Goodenough, "High-Resolution ADCs Up Dynamic Range in More Applications," Electronic Design, 11 Apr 91, pp. 65-79.

14) M. Story, "Oversampling ADCs," 7 Jun 90 (unpublished).

15) J. C. Candy, "A Use of Limit Cycle Oscillations to Obtain Robust Analog-to-Digital Converters," IEEE Trans. on Communications, Vol. 22, No. 3, Mar 74, pp. 298-305.

16) B. P. Agrawal and K. Shenoi, "Design Methodology for Sigma-Delta Modulator," IEEE Trans. on Communications, Vol. 31, No. 3, Mar 83, pp. 360-369.

17) M. W. Hauser and R. W. Brodersen, "Circuit and Technology Considerations for MOS Delta-Sigma A/D Converters," in Proceedings of the International Symposium on Circuits and Systems, San Jose, CA, May 86, pp. 1310-1315.

18) A. Agnello, "16-Bit Conversion Paves the Way to High-Quality Audio for PCs," Electronic Design, 26 Jul 90, pp. 61-66.